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ADSP-TS20xS TigerSHARC® System Design Guidelines

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Introduction

This EE-Note discusses specific hardware issues when implementing a system design, which incorporates any of the ADSP-TS20xS TigerSHARC® processors. This document is provided as an aid to hardware engineers for designing systems using processors with silicon revisions of 1.0 and higher.

All of the guidelines provided in this EE-Note apply to ADSP-TS201S, ADSP-TS202S, and ADSP-TS203S TigerSHARC embedded processors.

Power Supplies

The ADSP-TS20xS processor has four power supply domains V_{DD} (Internal), V_{DD_A} (Analog PLL), V_{DD_IO} (External I/O) and a V_{DD_DRAM} (DRAM) domain. The V_{DD_A} supply is a filtered version of the V_{DD} supply.

Refer to the *ADSP-TS20xS TigerSHARC Embedded Processor Data Sheet* [1] for more specific details.

- **V_{DD} Power Supply**

  The V_{DD} power supply pins are used to power all internal logic except for the internal DRAM, I/O's and PLL.

- **V_{DD_A} Power Supply**

  The two V_{DD_A} power supply pins are used to directly power the PLL. These pins are isolated from the internal V_{DD} supply pins so additional decoupling and filtering circuits can be added to reduce noise.

  For multiprocessor designs ADI recommends keeping the V_{DD_A} supplies separate for each processor. Refer to the V_{DD_A} supply decoupling section for further details.

- **V_{DD_IO} Power Supply**

  The V_{DD_IO} power supply pins provide power to all the I/O's including all the link port LVDS pins.

- **V_{DD_DRAM} Power Supply**

  The V_{DD_DRAM} power supply pins provide power to the internal embedded DRAM logic.

Ground (V_{SS}) Supply

The ADSP-TS20xS processor contains a single ground supply V_{SS}. The V_{SS} pins are ground returns for the V_{DD}, V_{DD_A}, V_{DD_DRAM} and V_{DD_IO} supply pins.

Power Supply Current

The V_{DD}, V_{DD_A}, V_{DD_DRAM} and V_{DD_IO} power supply currents can be calculated with the formulas specified in the application note *Estimating Power For The ADSP-TS201S (EE-170)* [5].

Power Supply Sequencing

There are no power sequencing requirements other than the V_{DD_DRAM} voltage *must* occur last. Refer to the *ADSP-TS201S TigerSHARC Embedded Processor Data Sheet* [1] for more information.

Supply Bypass Capacitors

The ADSP-TS20xS processor requires bypass capacitors on each supply. In many cases it is difficult to place lots of supply bypass capacitors close to the package pins, especially on the bottom side of the PCB. ADI recommends that PCB designers prioritize decoupling capacitor placement in the following order:

1. V_{DD_A} to V_{SS} bypass capacitors
2. V_{DD} to V_{SS} bypass capacitors
3. V_{DD_DRAM} to V_{SS} bypass capacitors
4. V_{DD_IO} to V_{SS} bypass capacitors

Low-ESR/low-ESL 0.1 µF capacitors are recommended for proper bypassing. For higher-frequency filtering, 0.01 µF and 0.001 µF capacitors can also be used (in

addition to the 0.1 µF capacitors), provided their inductance is small enough. In some cases, performing SPICE analyses of the power supply filtering characteristics may be necessary.

Enough "bulk" capacitors must be used to prevent power supply ripple that exceeds max/min power supply tolerances (*refer to the data sheet for the appropriate supply tolerances*) caused by current transients in the system. Several parallel electrolytic and/or tantalum capacitors are preferred in order to minimize ESR and to provide sufficient capacitance.

V_{DD_A} Supply Decoupling

The two analog (V_{DD_A}) supply pins power the clock generator PLLs. To produce a good stable clock, systems must provide a "clean" power supply to the V_{DD_A} domain. Therefore, the system designer must pay critical attention to bypassing and filtering of the V_{DD_A} supply. The decoupling capacitor placement for V_{DD_A} should be given first priority over the other supplies. Figure-1 shows the recommended design of the V_{DD_A} filtering circuit. The components used in this circuit should be placed as close as possible to the V_{DD_A} pins to minimize inductance and stray capacitance.

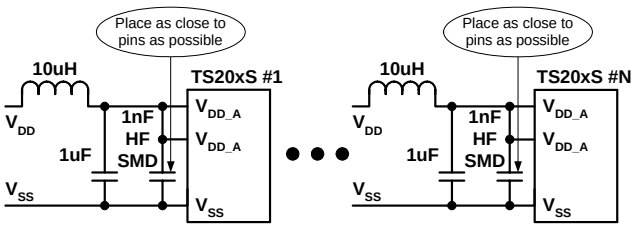

Figure-1: V_{DD_A} Supply Decoupling

It is recommended that the V_{DD_A} decoupling circuit be duplicated for each processor in multiprocessor systems.

- Place 10 µH inductor and 1 µF capacitor together with good connections to V_{DD}, V_{SS}, and V_{DD_A}.
- Place one (minimum) or two 1 nF HF SMD capacitors as close to the V_{SS} and V_{DD_A} package pins as possible.
- Make sure that the V_{DD_A} PCB trace isn't close to any noise-generating signals.

V_{DD_DRAM} Supply Decoupling

Below are the minimal recommended bypass capacitor requirements for a single processor's V_{DD_DRAM} supply. All capacitors should be duplicated for each processor in the system.

1. Minimum of six 1 nF high frequency bypass capacitors located as close to the package pins as possible.
2. At least two 10 nF bypass capacitor located as close to the package pins as possible.
3. At least four 0.1 µF bypass capacitors located as close to the package pins as possible.
4. A minimum of 47 µF of "bulk" low ESR (less then 100mΩ) capacitors for each processor connected to the V_{DD_DRAM} supply is recommended. These capacitors are used to reduce power supply ripple during high peak transient currents.
    - Single Electrolytic: Panasonic FK Series or Sanyo OS-CON series
    - Single tantalum: AVX TPS III series
    - Multiple ganged MLC capacitors: AVX Y5V series

V_{DD} Supply Decoupling

High frequency noise on internal supplies can adversely affect the speed of any device. It is always important to provide robust supply bypassing for internal supplies especially for products whose internal voltages are less than 1.5 V. It is recommended that as many high-frequency capacitors as possible be connected to the V_{DD} supplies as close to the package pins as possible.

A minimum of 470 µF of "bulk" low ESR (less than 25 mΩ) capacitors for each processor connected to the V_{DD} supply is recommended. These capacitors are used to reduce power supply ripple during high peak transient currents.

1. Minimum of six 1 nF high frequency bypass capacitors located as close to the package pins as possible.
2. At least two 10 nF bypass capacitor located as close to the package pins as possible.
3. At least four 0.1 µF bypass capacitors located as close to the package pins as possible.
4. A minimum of 470 µF of "bulk" low ESR (less than 25 mΩ) capacitors for each processor connected to the V_{DD} supply is recommended. These capacitors are used to reduce power supply ripple during high peak transient currents.

- Single Electrolytic: Panasonic FK Series or Sanyo OS-CON series
- Single tantalum: AVX TPS III series
- Multiple ganged MLC capacitors: AVX Y5V series

Proper V_{DD} supply design is critical to ensure operation within the data sheet specifications under *all* operating conditions. Adhering to the data sheet V_{DD} and I_{DD} specifications will ensure that no run time system errors will occur due to specification violations.

V_{DD_IO} Supply Decoupling

It is important to provide proper decoupling on the V_{DD_IO} supply. Although not as important as the V_{DD_A}, V_{DD}, and V_{DD_DRAM} supplies, careful capacitor placement and supply ripple analysis is required to ensure adequate decoupling.

1. Minimum of six 1 nF high frequency bypass capacitors located as close to the package pins as possible.
2. At least two 10 nF bypass capacitor located as close to the package pins as possible.
3. At least four 0.1 µF bypass capacitors located as close to the package pins as possible.
4. A minimum of 100 µF of "bulk" low ESR (less than 100 mΩ) capacitors for each processor connected to the V_{DD_IO} supply is recommended. These capacitors are used to reduce power supply ripple during high peak transient currents.
   - Single Electrolytic: Panasonic FK Series or Sanyo OS-CON series
   - Single tantalum: AVX TPS III series
   - Multiple MLC capacitors: AVX Y5V series

V_{REF} Pin

The ADSP-TS20xS contains a single V_{REF} voltage reference pin. This pin sets the input reference voltage for certain input pins. For the exact list of pins whose threshold is set by V_{REF} refer to the *ADSP-TS201S TigerSHARC Embedded Processor Data Sheet* [1].

The V_{REF} voltage should be set to the value specified in the data sheet with recommended circuit in Figure-2 below. All resistor tolerances must be 1%. (For values of R1 and R2, refer to Figure 6 of the *ADSP-TS201S TigerSHARC Embedded Processor Data Sheet* [1].)

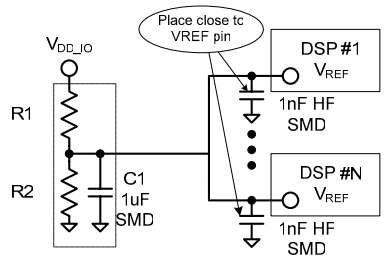

Figure-2: Recommended V_{REF} circuit

In multiprocessor (cluster bus) designs V_{REF} should be shared between all DSPs. It is important to make sure that each processor has at least one (preferably more) 1 nF high speed decoupling capacitor located close to the V_{REF} pin. It is also important to keep noise sources from coupling into the V_{REF} signal.

SCLK_V_{REF} Pin

The ADSP-TS20xS contains a single SCLK_V_{REF} voltage reference pin. This pin sets the input reference voltage for the SCLK input pin.

The SCLK_V_{REF} voltage should be set to the value specified in the data sheet with the recommended circuit in Figure-3. All resistor tolerances must be 1%. (For values of R1 and R2, refer to Figure 7 of the *ADSP-TS201S TigerSHARC Embedded Processor Data Sheet* [1].)

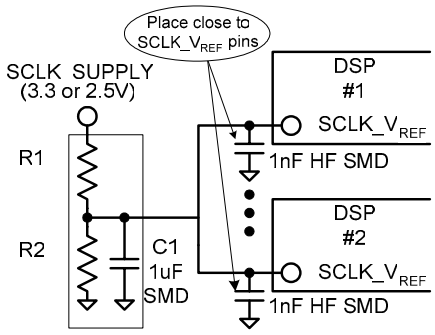

Figure-3: Recommended SCLK_V_{REF} circuit

In multiprocessor (cluster bus) designs, SCLK_V_{REF} should be shared between all DSPs. It is important to make sure that each processor has at least one (preferably more) 1 nF high speed decoupling capacitor located close to the SCLK_V_{REF} pin. It is also important to keep any noise source from coupling into the SCLK_V_{REF} signal.

No-Connect (NC) Pins

The ADSP-TS20xS contains several No-Connect (NC) pins. These pins ***must*** not connect to any supply or ground (V_{DD}, V_{DD_IO}, V_{DD_A}, V_{DD_DRAM}, or V_{SS}) and they must not connect to any other NC pin. All NC pins must be left totally unconnected.

Configuration Pins

The ADSP-TS20xS configuration pins SCLKRAT2-0, ID2-0, CONTROLIMP1-0 and DS2-0 are used to select various chip functions such as PLL clock ratio, chip-ID and output impedance. These pins typically have either an internal pull-up or pull-down resistor. All configuration pins *must* have a constant value while the ADSP-TS20xS is powered.

When using the default configuration, no external connection is needed; the pin should be treated as a NC (No Connect). For all other configurations (non default), the pin must be connected to V_{DD_IO} or V_{SS} directly or through a sufficiently strong resistor.

In multi-processor designs where configuration pins are likely to be wired together (SCLKRAT2-0 connected to several processor's) make sure that a proper value of resistor is used to override the default pull-down/up. Note that the total resistor value is divided by the number of processors.

For initial or prototype designs it is advantageous to have pads on the PCB for populating strap resistors to change the default setting for all the SCLKRAT2-0, CONTROLIMP1-0 and DS2-0 pins. Configuration pins, which have default pull-ups, should have resistor pads between the pin and V_{SS} and default pull-downs should have resistor pads between the pin and V_{DD_IO}.

- **CONTROLIMP1-0 Configuration Pins**

  The CONTROLIMP0 pin has an internal pull-down resistor and CONTROLIMP1 has an internal pull-up resistor. These pins control output driver impedance. Refer to Table 12 of the *ADSP-TS201S TigerSHARC Embedded Processor Data Sheet* [1] for more information on the CONTROLIMP1-0 pin values.

  

  For all designs it is recommended to set the CONTROLIMP1-0 pins to a value of "00" (Normal), since this is the only mode supported by IBIS model simulation.

- **DS2-0 Configuration Pins**

  The DS2 and DS0 pins contain an internal pull-up resistor. DS1 contains an internal pull-down resistor. These pins control the drive strength of the ADSP-TS20xS output drivers. For further information refer to the *ADSP-TS201S TigerSHARC Embedded Processor Data Sheet* [1] and the application note *User Guide to ADSP-TS201S TigerSHARC processor IBIS files (EE-198)* [7].

- **SCLKRAT2-0 Configuration Pins**

  The SCLKRAT2-0 pins contain an internal pull-down resistor. These pins set the PLL multiplier, which generates the core clock from the SCLK input.

  For more information on the maximum SCLK duty cycle specifications, and max/min SCLK frequency specifications, refer to the *ADSP-TS201S TigerSHARC Embedded Processor Data Sheet* [1].

- **ID2-0 Configuration Pins**

  The ID2-0 pins have an internal pull-down resistor. In single processor systems and in multiprocessor designs where the cluster bus is not connected to any other TS20xS device, the ID pins should be set to the default value (000). This is because internal pull-up/pull-downs on certain pins, like memory interface and bus arbitration are enabled only when the ID2-0 = (000). Setting the processor ID2-0 pins to (000) eliminates the need for external resistors. Refer to *ADSP-TS201S TigerSHARC Embedded Processor Data Sheet* [1] for more details.

  Note that ID2-0=[000] is the only processor which can enable SDRAM and start the MRS sequence.

  In multiprocessor designs where the cluster bus is shared between TS20xS devices, each processor must be programmed to a unique device ID starting with ID2-0 = (000) and incrementing upwards. The table and figures below describe the various configurations and ID2-0 assignments.

ID2-0	Multiprocessor ID
000 (default)	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

Table-1: ID2-0 Configuration options

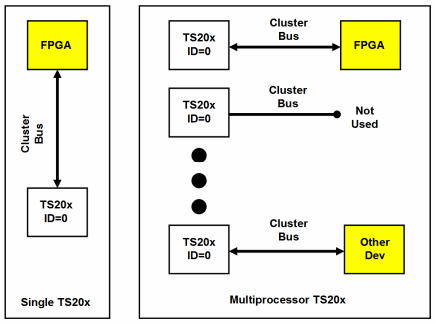

Figure-4: No cluster bus connection between TS20x processors. (All processor ID's must be 0)

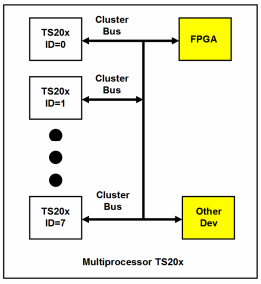

Figure-5: Cluster bus connection between TS20x processors. (All processor ID's must be unique)

Strap Pins: /BMS,/BM,TMR0E,/BUSLOCK

The ADSP-TS20xS processor contains four dual-purpose strap pins /BMS, /BM, TMR0E and /BUSLOCK. These strap pins select the boot-mode, SYSCON/SDRCON write enable, link port width and interrupt (edge/level). These strap pins also have additional functionality after reset.

When the default configuration is used, no external resistor is needed. For all other configurations, a sufficiently strong resistor (typically 500 Ω) connected to V_{DD_IO} is required. Do not strap these pins directly to any supply or any other pin.

For designs which are driving strap pins directly from an FPGA, ASIC or other device, refer to the data sheet for timing details on when the strap pins are sampled and when the FPGA, ASIC or device should stop driving strap pin data value.

The four strap pins have an internal pull-down resistor, pull-up resistor or no-resistor (three-state) on each pin. The resistor type, which is connected to the I/O pad, depends on whether /RST_IN is active (low) or if /RST_IN is de-asserted (high). Refer to Table 17 ("Strap Pin Internal Resistors") of the *ADSP-TS201S TigerSHARC Embedded Processor Data Sheet* [1] for more information.

- **/BMS Strap Pin (EBOOT)**

  The /BMS strap pin sets EEPROM (default) or External boot mode.

  During reset, /RST_IN (low), a 5 kΩ pull-down resistor is enabled on /BMS if the chip's ID2-0 pins are programmed to (000). All remaining DSPs ID2-0 programmed to (1 to 7), in the system, will not have any pull-downs or pull-ups active on /BMS.

  To over-ride the default setting, place a sufficiently strong resistor (typically 500 Ω) between /BMS and V_{DD_IO}.

/BMS	Boot Mode
0 (default)	EPROM Boot
1	External or Link port Boot

Table-2: /BMS strap options

- **/BM Strap Pin (IRQEN)**

  The /BM strap pin sets Interrupt disable (default) or Interrupt enable for /IRQ3-0. During reset, /RST_IN (low), an internal pull-down resistor is enabled.

  To override the default setting, place a sufficiently strong resistor (typically 500 Ω) between /BM and V_{DD_IO}.

/BM	Interrupt Enable, (IRQ3-0) Type
0 (default)	Disable interrupts, level-sensitive
1	Enable interrupts, edge-sensitive

Table-3: /BM strap options

If the /BM and /BMS strap pins are high, at the de-assertion of /RST_IN, the processor starts running from the memory address selected by one of the /IRQ3-0 signals (one /IRQ signals should be asserted). The table below shows the starting memory address.

Interrupt	Address
/IRQ0	0x3000 0000 (External Memory, /MS0)
/IRQ1	0x3800 0000 (External Memory, /MS1)
/IRQ2	0x8000 0000 (External Memory, /MSH)
/IRQ3	0x0000 0000 (Internal Memory)

Table-4: No Boot, Run From Memory Address

- **TMR0E Strap Pin (LINK_DWIDTH)**

  The TMR0E strap pin sets the Link Port Data Width, 1-bit (default) or 4-bit, for all Link Ports. During reset, /RST_IN (low), an internal pull-down resistor is enabled on the TMR0E pin.

  To override the default setting, place a sufficiently strong resistor (typically 500 Ω) between TMR0E and V_{DD_IO}.

TMR0E	Link Port Input Data Width
0 (default)	1-Bit
1	4-bit

Table-5: TMR0E strap options

- **/BUSLOCK Strap Pin (/SYS_REG_WE)**

  The /BUSLOCK strap pin sets the write enable to always writable or one-time writable (default) for the SYSCON and SDRCON registers.

  During reset, /RST_IN (low), an internal pull-down resistor is enabled on the /BUSLOCK pin if the chip's processor ID is programmed to "0". All remaining processor ID's (1-7), in the system, will not have any pull-downs or pull-ups active on /BUSLOCK.

  To over-ride the default, place a sufficiently strong resistor (typically 500 Ω) between /BUSLOCK and V_{DD_IO}.

/BUSLOCK	SYSCON/SDRCON write enable
0 (default)	One-time writable after reset
1	Always writable

Table-6: /BUSLOCK strap options

Test Mode Strap Pins (Link Port)

There are three special test strap pins /L1BCMPO, /L2BCMPO and /L3BCMPO, which enable test mode functions. These pins are the Link Port 1, 2, and 3's Block Completion signals. They are normally outputs, however, when /RST_IN is active (low) these pins are three-stated and an internal pull-up resistor enabled.

All FPGAs and some ASICs three-state their pins before they are programmed. During this time, some FPGAs and/or ASICs typically turn on an internal pull-up or pull-down resistor. These resistors are used to keep signals from floating to mid-scale before programming. It is important to make sure that the FPGA or ASIC which connects to Link Port 1, 2, or 3's Block Completion pins don't have any internal pull-down resistor active while /RST_IN is asserted (low). If the FPGA or ASIC has a pull-up this is ok.

Note, only link ports 1, 2, and 3 have special test mode straps. If only one link port requires connection to an FPGA or ASIC, use link port "0" since this Link Port Block Completion signal doesn't have any test mode straps associated with it.

For designs which are driving Test Mode strap pins directly from an FPGA, ASIC or other device, refer to the data sheet for timing details on when the Test Mode strap pins are sampled and when the FPGA, ASIC or device should stop driving strap pin data value.

Note: If under any circumstances, at the rising edge of reset (de-assertion edge), if any of the 3 test mode Block Completion signals has a value other than a logic-1 a processor test mode will be enabled.

To assist in debugging it is recommend that designers include an option for placing three optional pull-down resistors (typically 500 Ω) between the Test Mode Strap pins and V_{SS}. It is also recommended that designers include an option for placing three optional pull-up resistors (typically 500 Ω) between the Test Mode Strap pins and V_{DD_IO}. These resistors can be added or removed to enable and disable each specific test modes.

Test Mode Description	Strap Pin
TM1	/L1BCMPO
TM2	/L2BCMPO
TM3 • CCLK/4 on pin /L0BCMPO • SOCCLK/2 on pin /L1BCMPO • SCLK on pin /L2BCMPO	/L3BCMPO

Table-7: Link Port test mode strap options TS201/TS202

Test Mode Description	Strap Pin
TM1	/L1BCMPO
TM2	TM2
TM3 • CCLK/4 on pin /L0BCMPO • SOCCLK/2 on pin /L1BCMPO • SCLK on pin TM2	TM3

Table-8: Link Port test mode strap options TS203

SCLK Pin

After power-up the SCLK signal should not stop running unless the reset signal (/RST_IN) is asserted. If SCLK needs to stop following the power-up sequence, /RST_IN must also get asserted. When re-starting the SCLK from this condition, follow the same guidelines as the power-up sequence.

SCLK Distribution

In single and multiprocessor designs careful clock design and distribution is required to ensure proper and full-speed internal and external operation.

Listed below are some guidelines for clock distribution.

- PCB connections should be point-to-point from the clock buffer output to all clock inputs. Trace lengths should be matched (+/- 125 mils) to minimize skew.
- Capacitance on all clock signals should be matched within 5%.
- Minimize the number of PCB vias.
- Maintain same number of vias on each clock signal.
- Do not run clock signals close to other signals on same layer. Keep at least 4x minimum spacing to other signals.
- Do not run any signals directly above or below the clock signals.
- Use a high quality low-jitter clock source for generating the clock reference.
- Use a low-jitter clock buffer driver.
- Use a low output-to-output skew clock buffer driver.
- All clock signals from the clock buffer outputs to the SCLK inputs should be carefully reviewed.
- A single, multiple-output clock buffer should be used to drive the clock signals to all devices including DSPs, FPGAs, ASICs and Memories. Using multiple clock buffer chips increases the clock-to-clock skew between clock signals and is not recommended.

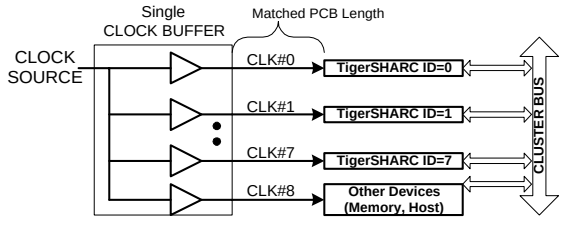

Figure-6: Recommended Clock Distribution Method

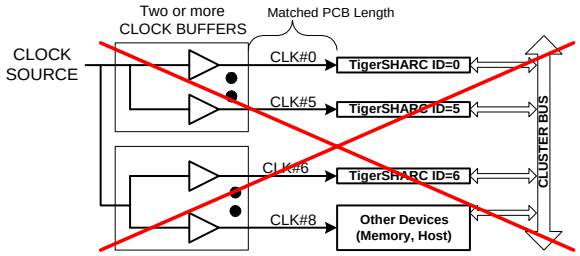

Figure-7: Not Recommended Clock Distribution Method

SCLK Design Considerations

Careful analysis is required when choosing components for generating, buffering and distributing the SCLK signals on a PCB. Refer to the ADSP-TS20xS data sheet specification for SCLK input jitter requirements.

Single-stage or dual-stage clock tree designs are typically used to create a clock distribution network. Figure-8 shows a couple of examples of these types of designs.

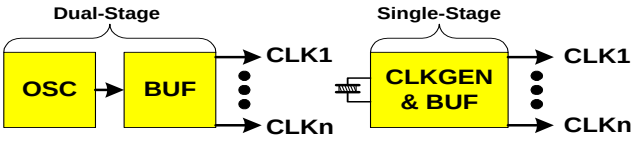

Figure-8: Clock Generation Examples

In most instances single stage clock designs provide lower jitter specifications and tighter duty-cycle control than dual or multi-stage clock designs. It is very important to simulate all designs, however dual and multi-stage designs require special attention when analyzing total jitter (OSC jitter & BUF jitter) and duty cycle impact. In some cases jitter is additive, therefore a 100 ps OSC jitter + 150 ps BUF jitter could result in a 250 ps total peak-to-peak jitter. In some BUF products, however, some input jitter is filtered out resulting in only a fraction of the input jitter being added to the inherent BUF jitter. Designers should review manufacturer data sheets and application notes before choosing Oscillators, Crystals and clock driver components to ensure they meet the jitter, rise/fall time, and duty cycle requirements for the SCLK of the ADSP-TS20xS.

It is important to ensure that the SCLK_V_{REF} reference voltage complies with the data sheet specification. It is important to note that the duty cycle of SCLK is dependent upon the SCLK_V_{REF} voltage setting.

Other factors to consider: When selecting components, the output-to-output skew between various clock buffer outputs should be as small as possible to ensure high speed operation of the external bus interface. Make sure the

output rise and fall times of clock drivers are symmetrical. Review power supply grid and supply decoupling for all clock generation components. Signal integrity analysis should be run on all clock signals to ensure no external coupling and they meet or exceed the SCLK specifications.

Reset Pins

There are four external pins /RST_IN, /RST_OUT, /POR_IN and /TRST associated with the reset circuitry of the ADSP-TS20xS. Three of the pins /RST_IN, /RST_OUT and /POR_IN are associated with resetting the core and internal DRAM. These pins ***must*** be configured as shown in Figure-11 below. The /TRST pin is the JTAG and Emulator reset pin.

ADI recommends designers place a 0 Ω resistor between /RST_OUT and /POR_IN. This provides a useful place for connecting a trigger to a logic-analyzer or oscilloscope for debugging potential system problems.

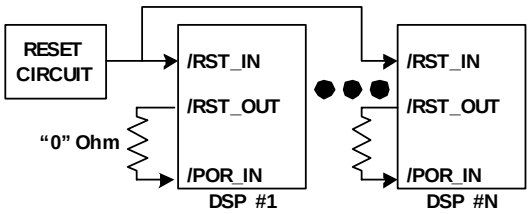

Figure-9: Hardware Reset Pin Connections

/RST_IN is the chip hardware reset pin, /RST_OUT is a delayed and synchronized internal version of /RST_IN and /POR_IN is used to reset the internal DRAM.

In multiprocessor designs, the /RST_IN signal must be connected to all devices to provide a common reset sequence. Each processor should connect its /RST_OUT pin to its /POR_IN pin.

It is required that the circuit supplying /RST_IN should hold the signal asserted (low) when the power supply is ramping up to its stable value.

The TS20xS has four types of resets; Power-Up Reset, Normal Reset, Core Reset and JTAG/Emulator Reset.

- **Power-Up Reset:**

  Refer to the "Power-Up Reset Timing" and "Normal Reset Timing" sections of the *ADSP-TS201S TigerSHARC Embedded Processor Data Sheet* [1] for specific timing on the /RST_IN and SCLK pins.

  All strap and test mode pins are sampled 14 SCLK cycles *after* /RST_IN is de-asserted. Refer to the *ADSP-TS201S TigerSHARC Embedded Processor Data Sheet* [1] for exact timing when theses pins are latched.

- **Normal Reset**

  Normal Reset is defined as any chip reset (assertion of /RST_IN) following the initial Power-Up Reset. The supplies, SCLK and other signals must be stable.

- **Core Reset:**

  When setting the SWRST bit in the register EMUCTL, the processor core is reset, but not the external ports or I/O. This is sometimes referred to as a software reset.

- **/TRST Boundary Scan and Emulator Reset:**

  The /TRST reset pin not only resets the IEEE 1149.1 Boundary Scan port but it also provides the reset signal for the Emulator interface. This signal requires special considerations if the Emulator or Boundary Scan port is being used.

  Refer to EE-68 *"Analog Devices JTAG Emulation Technical Reference"* [4] for more information.

Boundary Scan and Emulator Pins

The ADSP-TS20xS has six pins associated with the Boundary Scan and Emulator interface. The pins, /EMU, TCK, TDI, TDO, TMS and /TRST should be connected to a Boundary Scan pod connector if the ADSP-TS20xS emulator is used. To get detailed and updated information on this subject, please refer to engineering note *Analog Devices JTAG Emulation Technical Reference (EE-68)* [4].

Cluster Bus Pins

In a single processor system, the ID2-0 pins of the single processor *must* be set to "000". In a multiprocessor system, the processor IDs must be uniquely assigned starting from "000" up to "111"; a single TigerSHARC cluster can gluelessly support up to 8 DSPs. For both single and multiple processor topologies, it is imperative to include processor ID2-0 = "000" in the system, since this processor supports the following features upon reset:

- Has active internal pull-ups or pull-downs on certain external signals when ID2-0="000" (processor ID 0). See *ADSP-TS201S TigerSHARC Embedded Processor Data Sheet* [1] for details.

- Is the default bus master, and can therefore provide active bus arbitration signals to an external host processor.
- Has an on-chip SDRAM controller, which provides an MRS sequence to any external SDRAM present in the system.

If there is an external host on the cluster bus and common data are shared between the host and the TigerSHARC processor(s), the endianess on both sides must be matched to each other. Note, the TigerSHARC processor is only little endian and does not support big endian.

The TigerSHARC processor's addressing is word-oriented (32-bit). Some host processors' addressing is byte-oriented. Therefore, for connecting to these processors the least-significant bit of the TigerSHARC processor's address bus should be connected to the third least-significant bit of the host processor's address bus, regardless if a 32-bit or 64-bit bus width is specified.

The address and data busses may float for several cycles during bus-mastership transitions between a TigerSHARC processor and a host. Floating in this case means that these inputs are not driven by any source. The ADSP-TS20xS contains internal pull-up resistors to ensure busses don't float under these conditions.

If either the host or external memory bus widths are configured as 64-bits, then the multiprocessing memory space must be configured as 64-bits as well. If external wait-state mode is used, please ensure that no contention on the ACK signal occurs.

Link Ports Pins

The ADSP-TS201S and ADSP-TS202S contain four full-duplex Link Ports, whereas the ADSP-TS203S contains only two full-duplex Link Ports. Each link port's receive and transmit sections operate independently and may or may not be used or connected to other link partners. If link ports are used then all link port pins must be connected between link partners. The only exception is for 1-bit data mode operation. Refer to the following sections for connecting or terminating the transmit and receive link port.

The Link Ports on revision 1.2 silicon have a 100 Ω terminating resistor across the LVDS P/N clock and data pin pairs, on the link port input pins (i.e. the receiver pin pairs), incorporated on-chip. Therefore, an external 100Ω terminating resistor is no longer required on the PCB.

Systems that will be populated with revision 1.0 or 1.1 of ADSP-TS20x silicon, must be designed to use external 100 Ω termination resistors. This will also allow the use of revision 1.2 silicon on the same PCB, by simply removing this resistor. Systems that will be populated with *only* revision 1.2 silicon (and newer), do not need to be designed for the external resistors.

Transmit Link Port Connections

Transmit link port connections should follow guidelines in the tables below. Note that the /LxBCMPO pins for transmit link ports 1, 2 and 3 can be used for test mode straps. Refer to the test mode strap section for details. In cases where only one data transmit signal pair is used, the remaining 3 transmit pairs should be left unconnected or terminated with 100Ω resistors as shown in Table-10.

Pin Name	Pin Connection
LxDATAO3-0P/N	Link Partner
LxCLKOUTP/N	Link Partner
LxACKI	Link Partner
/LxBCMPO	Link Partner *

Table-9: 4-bit Transmit Link Port

Pin Name	Pin Connection
LxDATAO3-1P/N	NC
LxDATAO0P/N	Link Partner
LxCLKOUTP/N	Link Partner
LxACKI	Link Partner
/LxBCMPO	Link Partner*

Table-10: 1-bit Transmit Link Port

Pin Name	Pin Connection
LxDATAO3-0P/N	NC
LxCLKOUTP/N	NC
LxACKI	NC
/LxBCMPO	NC*

Table-11: Unused Transmit Link Port

*: Refer to Test Mode strap section for information on providing PCB pads for optional resistor placement for system debug.

- **Receive Link Port Connections**

Receive link port connections should follow guidelines in the tables below. If a receive link port is used, all pins must be connected with the exception of the 3 data pins when using a 1-bit wide data port.

For silicon revisions 1.0 and 1.1, each LVDS receive pair that is connected to a link partner requires an external 100 Ω 1% terminating resistor. These resistors must be placed as close to the receiving link port pins as possible.

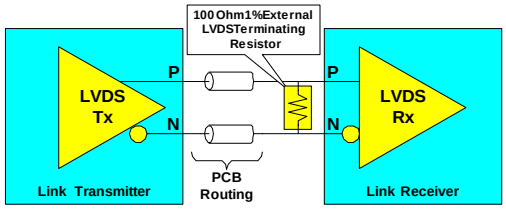

Figure-10: LVDS Receive Termination (for silicon revisions 1.0 and 1.1)

For silicon revisions 1.2 and newer, the external 100Ω 1% terminating resistor is not required.

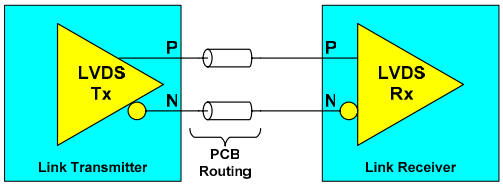

Figure-11: LVDS Receive Termination (for silicon revisions 1.2 and newer)

Pin Name	Pin Connection	Termination Resistor
LxDATAI3-0P/N	Link Partner	Yes*
LxCLKINP/N	Link Partner	Yes*
LxACKO	Link Partner	N/A
/LxBCMPI	Link Partner	N/A

Table-12: 4-bit Receive Link Port

Pin Name	Pin Connection	Termination Resistor
LxDATAI3-1P/N	V_{DD_IO}	No
LxDATAI0P/N	Link Partner	Yes*
LxCLKINP/N	Link Partner	Yes*
LxACKO	Link Partner	N/A
/LxBCMPI	Link Partner	N/A

Table-13: 1-bit Receive Link Port

Pin Name	Pin Connection	Termination Resistor
LxDATAI3-0P/N	V_{DD_IO}	No
LxCLKINP/N	V_{DD_IO}	No
LxACKO	NC	N/A
/LxBCMPI	NC or V_{SS}	N/A

Table-14: Unused Receive Link Port

*The receive link ports on revision 1.2 silicon does not require any external terminating resistors.

- **Using Connectors for Link Port Communication**

Some applications may require either daughter-cards or cable connectors for communications between link ports on separate systems. This requires special considerations for inputs when the cable or perhaps daughter-board is not used or plugged in.

The following guidelines should be followed when using connectors:

- LxDATAO3-0P/N, LxCLKOUTP/N, LxBCMPO and LxACKO; these outputs should be connected to the connector or left unconnected if not used (for example using only 1-bit data).
- LxDATAI3:0P/N and LxCLKINP/N; these differential inputs require an input termination resistor located close to the receiver pins if they are used. (For silicon revision 1.2 and newer, this external input termination resistor is not required.)
- LxACKI; this signal has an internal pull-down resistor. No special requirements needed.
- /LxBCMPI; this signal has an internal pull-up resistor. No special requirements needed.

Link Port LVDS PCB Guidelines

- PCB traces should be optimized for 100 Ω differential impedance.
- Connections should be point-to-point from the Link Port source to the Link Port destinations. Trace lengths should be matched to minimize skew. All trace lengths should be +/- 250 mils. This limits PCB trace delays to +/- 50 ps.
- For high-speed 4-bit Link Port operation, place the Link Port clock signals between the four sets of LVDS data signals

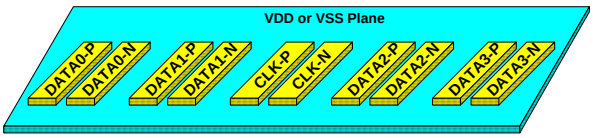

Figure-12: 4-Bit Link Port Clock placement

- Minimize the number of PCB vias. Vias reduce signal integrity. Additional stub length can cause unwanted reflections.
- No signals or vias between LVDS pairs.

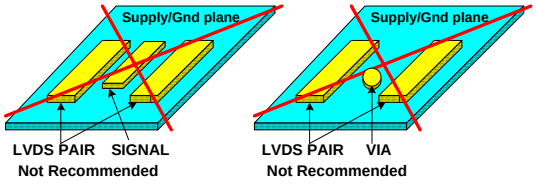

Figure-13: No Signals Between LVDS signal

- Do not place any closely spaced signals or vias between adjacent LVDS pairs unless careful analysis is done.

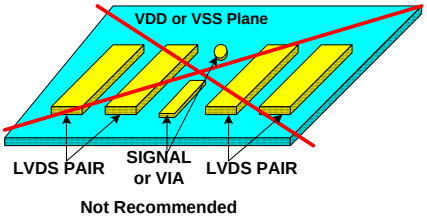

Figure-14: No Signals Between LVDS pairs

- No 90 degrees angles for LVDS routing. Use 45-degree bends and maintain constant width and space between all LVDS pairs and spacing between adjacent LVDS pairs.

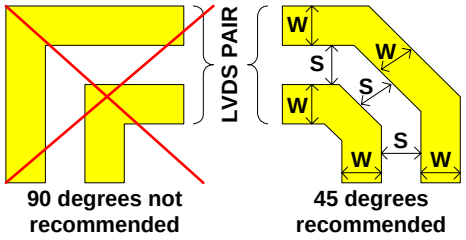

Figure-15: No 90-Deg Angles for LVDS signals

- Do not run any signals under or above LVDS pairs.

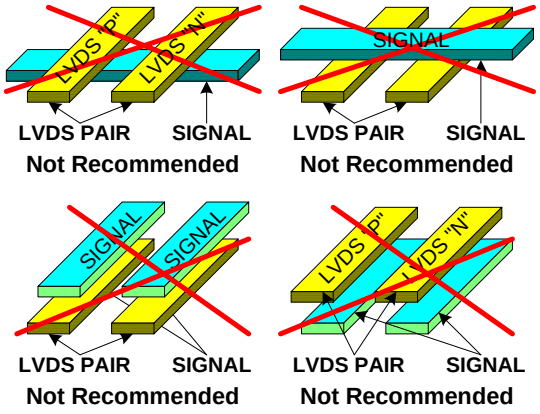

Figure-16: No Signals above/below LVDS signals

- Place LVDS differential signals on the top or bottom layer of the PCB if possible. A solid supply or ground plane directly underneath the LVDS signals is also required. This configuration is typically referred to as "MicroStrip".

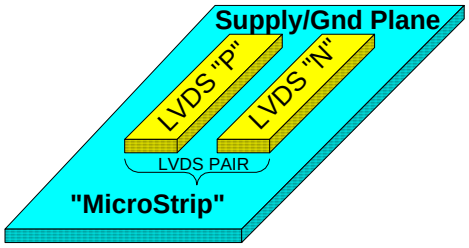

Figure-17: MicroStrip Example

- If placement of LVDS signals is not possible on the top or bottom layers of the PCB, it is acceptable to sandwich the LVDS layers in between supply and/or ground planes. This configuration is referred to as "StripLine".

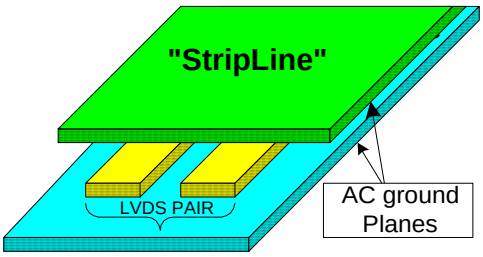

Figure-18: StripLine Example

Although the StripLine topology significantly reduces EMI, it does have some drawbacks.

1. Difficulty maintaining constant impedance
2. Higher propagation delay (~1 ½ times)
3. May require additional vias and layers

- It is recommended that the supply and/or ground plane extend past the edges of all LVDS signals.

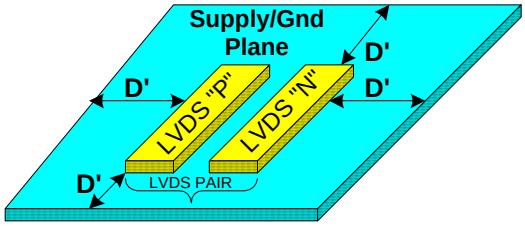

Figure-19: Supply Plane overlap of LVDS signal

- If a Non-LVDS (single ended) signal must run on the same plane as LVDS signals, a ground or supply trace should be inserted between the LVDS signal and the Non-LVDS signal.

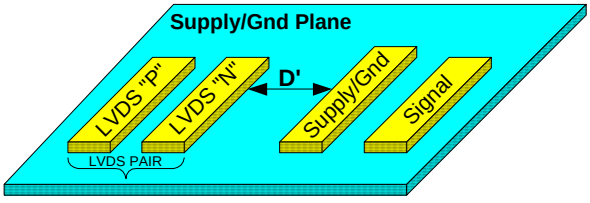

Figure-20: Non LVDS signal to LVDS distance

- Below are some industry standard guidelines for LVDS signal routing.

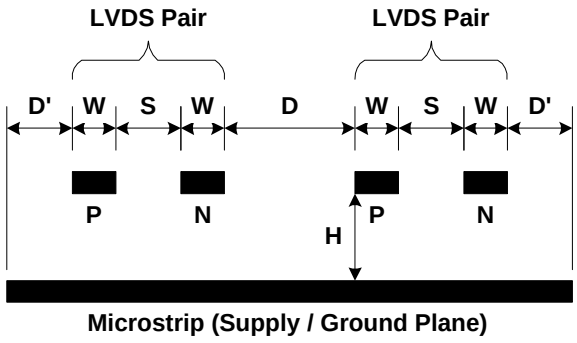

Figure-21: MicroStrip PCB guidelines

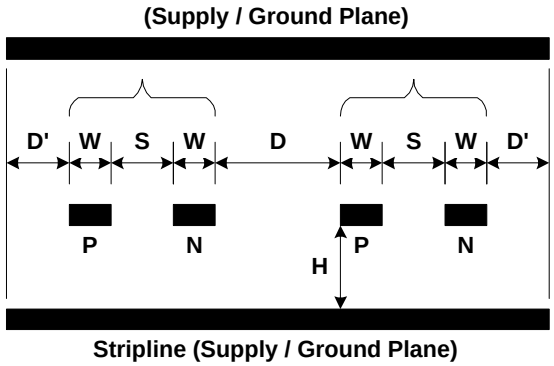

Figure-22: StripLine PCB guidelines

W = Width of PCB trace
S = Space between LVDS pair.
D = Distance between LVDS pairs
D' = Space to ground or supply plane edge
D' = Distance to neighboring supply trace
H = Height between signal and next layer

Note: The following PCB (S, D and H) Ratios are also required. Optimize the differential impedance of 100 Ω.

- S < 2W
- D, D' >= 2S
- H > S

Booting

To understand the booting process for each of the boot modes in further detail, please refer to TigerSHARC processor engineering note *ADSP-TS20x TigerSHARC Processor Boot Loader Kernels Operation (EE-200)* [8].

After reset, the ADSP-TS20xS has four boot options for beginning operation: EPROM Boot, Host Boot, Link Port Boot, and No Boot.

- **EPROM Boot:**
  Master Boot Mode, TigerSHARC processor starts actively fetching externally.
  The ADSP-TS20xS processor defaults to EPROM booting depending on the value of the /BMS strap pin. When the processor is configured to boot from EPROM, /BMS is active during the boot sequence and should be connected to the chip select signal of the EPROM. For additional information refer to the /BMS strap pin section.

- **Host Boot:**
  Slave Boot Mode: TigerSHARC processor expects code to be placed internally.
  The ADSP-TS20xS processor supports booting from an external master (host or another ADSP-TS20xS). Any master on the cluster bus can boot the ADSP-TS20xS through writes to its internal memory or through auto DMA.
  For host boot, place a sufficiently strong resistor (typically 500 Ω) between /BMS and V_{DD_IO}.

- **Link Port Boot:**
  Slave Boot Mode: TigerSHARC processor expects code to be placed internally.
  All four receive link port DMA channels are initialized after reset to transfer a 256-word block to internal memory addresses 0 through 255, and to issue an interrupt at the end of the block (similar to an external port DMA). The corresponding DMA interrupts are set to address zero. For additional information refer to the /BMS and TMR0E strap pin sections.
  For Link Port boot place a sufficiently strong resistor (typically 500 Ω) between /BMS and V_{DD_IO}.

- **No Boot:**
  Master mode: TigerSHARC processor will start from IRQ vector (externally or internally) fetching data.
  The ADSP-TS20xS processor will begin execution from the memory address selected with one of the /IRQ3-0 interrupt signals. Using the 'no boot' option, the ADSP-TS20xS will start running from memory when one of the interrupts is asserted. For additional information refer to the /BMS and /BM strap pin sections.
  For No boot (boot from memory address) place a sufficiently strong resistor (typically 500 Ω) between /BM to V_{DD_IO} and place a sufficiently strong resistor (typically 500 Ω) between /BMS to V_{DD_IO}.

Miscellaneous Items

- It is important to run PCB signal integrity analysis for all signals in a single or multiprocessor ADSP-TS20xS based systems.

References

[1] *ADSP-TS201S TigerSHARC Embedded Processor Data Sheet*, Analog Devices, Inc.

ADSP-TS202S TigerSHARC Embedded Processor Data Sheet, Analog Devices, Inc.

ADSP-TS203S TigerSHARC Embedded Processor Data Sheet, Analog Devices, Inc.

[2] *ADSP-TS201S TigerSHARC Processor Hardware Reference*, Analog Devices, Inc.

[3] *ADSP-TS201S TigerSHARC Processor Programming Reference*, Analog Devices, Inc.

[4] *Analog Devices JTAG Emulation Technical Reference (EE-68)*. Analog Devices, Inc.

[5] *Estimating Power For The ADSP-TS201S (EE-170)*, Analog Devices, Inc.

[6] *Thermal Relief Design for the ADSP-TS20xS TigerSHARC Processor (EE-182)*, Analog Devices, Inc.

[7] *User Guide to ADSP-TS201S TigerSHARC processor IBIS files (EE-198)*

[8] *ADSP-TS20x TigerSHARC Processor Boot Loader Kernels Operation (EE-200)*, Analog Devices, Inc.

[9] *Considerations for Porting Code from the ADSP-TS101S TigerSHARC Processor to the ADSP-TS201S TigerSHARC Processor (EE-205)*, Analog Devices, Inc.

Document History

Version	Description
Rev 4 – January 15, 2005 by Greg F.	Modified for production silicon. Updated link port section for rev 1.2 silicon. Updated SCLK_Vref information per data sheet spec
Rev 3 – May 19, 2003 by John A. & Phil G.	Discussing Rev 1.0 silicon
Rev 0.6 – October 23, 2003 by Phil G.	Revised title from *ADSP-TS201S TigerSHARC System Design Guidelines* to *ADSP-TS20xS TigerSHARC System Design Guidelines*
Rev 0.5 – October 22, 2003 by Greg F., John A. & Phil G.	First released version